ABSTRACT OF THE DISCLOSURE

A bi-directional serializer/de-serializer is disclosed using a single bi-directional data line and a single bi-directional clock line. Gated buffers are controlled to operate either sending or receiving data, and a phase locked loop provides a clock to shift data out from a shift register. A reference clock is supplied to the PLL and the PLL generates a synchronous bit clock. The bit clock is sent over the clock line in parallel with the serial data bits, and the PLL bit clock is synchronized to the data bits. Two data boundary bits are inserted between the word data bits, the boundary data bits are arranged with a logic level transition between the two data boundary bits. Also, at the boundary of the words during the sending of the two boundary data bits, the synchronous bit clock is arranged to have no logic level transition. The receiving system will use the bit clock to serial load the received word and boundary data bits into a shift register. When a word boundary is received, the two data boundary bits, the word boundary is detected by sensing a data bit transition while there is no bit clock transition.